# A 19-GHz Broadband Amplifier Using a $g_m$-Boosted Cascode in 0.18-$\mu$m CMOS

Masum Hossain and Anthony Chan Carusone
Edward S. Rogers Sr. Department of Electrical and Computer Engineering
University of Toronto
Email: masum@eecg.utoronto.ca, tcc@eecg.utoronto.ca

*Abstract*— **This paper describes a broadband CMOS amplifier for differential receiver front-ends. A capacitive cross-coupling network provides passive $g_m$-boosting in the input cascode stage. This results in a greater than 30% increase in bandwidth. Combined with several other established bandwidth-enhancement techniques, the prototype achieves a measured 3-dB bandwidth of 19 GHz with no peaking in a 0.18-$\mu$m CMOS process. The dc gain is 11 dB differential, and the power consumption is 113 mW. Eye diagrams up to 24 Gb/s are shown.**

## I. Introduction

Differential broadband communication receiver front-ends require amplifiers with flat magnitude response, linear phase response, and an input impedance matched to 50 Ω per side. This paper describes a multi-stage amplifier that combines several bandwidth-enhancement techniques to meet these requirements over a 19-GHz bandwidth in a 0.18-• m CMOS process.

Distributed amplifiers can be used as differential broadband low noise amplifiers in CMOS [1]. However, they require accurate passive device modeling to avoid ripple in the gain and group delay [2]. They can also consume considerable area.

CMOS cascodes are popular broadband amplifiers. Using inductive peaking and other techniques to distribute parasitic capacitances, the bandwidth of amplifiers based on cascode stages has been extended to 10 GHz in 0.18-• m CMOS [3], [4]. In [5] and [6], a cross-coupling capacitance was used to boost the transconductance of a differential common-gate amplifier in order to improve its noise figure. In this work, applying the same technique to the common-gate devices in a differential MOS cascode results in a greater than 30% improvement in bandwidth.

The • $_m$-boosted cascode is analyzed in Section II. In Section III, an input pre-amplifier employing the • $_m$-boosted cascode is described, including measurement results. Section IV describes a multi-stage amplifier that includes additional differential stages to increase the overall amplifier gain to 11 dB.

## II. Bandwidth-Enhancement Techniques for the MOS Cascode

A standard MOS cascode is shown in Fig. 1(a). Its bandwidth is determined by the time constants associated with the three nodes' parasitic capacitances: • $_{\mathrm{IN}}$, • $_{\mathrm{X}}$, and • $_{\mathrm{OUT}}$.

The input time constant is the product of the total input capacitance, • $_{\mathrm{IN}}$, and source resistance. Its effect can be reduced by inserting an inductance in series with the gate, • $_1$ in Fig. 1(b). This splits • $_{\mathrm{IN}}$ by separating the gate capacitance of • $_1$ from the output capacitance of the previous stage (or, as in this design, from the pad capacitance) [7].

The output time constant is the product of • $_{\mathrm{OUT}}$ and the amplifier's output resistance. Shunt and series peaking inductors, • $_3$ and • $_4$ in Fig. 1(b), can be used to improve the bandwidth at this node [8].

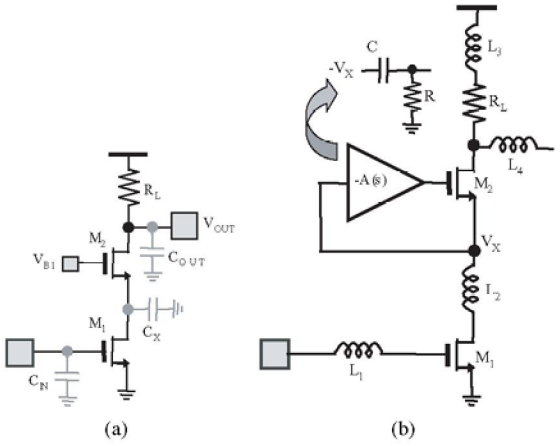



Fig. 1. (a) A conventional MOS cascode. (b) A $g_m$-boosted MOS cascode with enhanced bandwidth.

This leaves the time constant at the source of • $_2$, approximately • $_X$ • • $_{m2}$. Inserting inductor • $_2$ in Fig. 1(b) separates the drain capacitance of • $_1$ from the source capacitance of • $_2$ and, hence, improves the bandwidth at this node [3]. In this work, a feedback network, • (•), is introduced to increase the effective transconductance of • $_2$ providing a further bandwidth improvement.

Gain-boosting is a well-established technique that uses an amplifier in place of • (•) to increase the dc gain of a cascode stage. With negative feedback as shown in Fig. 1(b), the effective transconductance of • $_2$ is increased by a factor of [1 + • (•)],

$$\bullet_{m,\mathrm{eff}} = [1 + \bullet\ (\bullet)]\bullet_{m2}\bullet \tag{1}$$

In a fully-differential circuit, a cross-connection can be used to provide the negative polarity of the feedback. Using a simple CR-section for the cross-connection provides a first-order high-pass response,

$$\bullet\ (\bullet) = \frac{\bullet\ \bullet\ \bullet}{1 + \bullet\ \bullet\ \bullet}\bullet \tag{2}$$

Substituting (2) into (1) gives a frequency dependent transconductance,

$$\bullet_{m,\mathrm{eff}} = \frac{1 + 2\bullet\ \bullet\ \bullet}{1 + \bullet\ \bullet\ \bullet}\bullet_{m2}\bullet \tag{3}$$

Hence, at low frequencies • $\ll 1\bullet 4\bullet\ \bullet\ \bullet$ , • $_{m,\mathrm{eff}} \approx \bullet_{m2}$. Whereas, at high frequencies • $\gg 1\bullet 2\bullet\ \bullet\ \bullet$ , • $_{m,\mathrm{eff}} \approx 2\bullet_{m2}$. The result is a 6-dB • $_m$-boost at high frequencies, which reduces the effect of the time constant at the source of • $_2$ and, hence, extends the amplifier bandwidth

Capacitive cross-coupling has previously been used to reduce the noise factor of a CMOS common-gate stage [5], [6]. Here, it is being

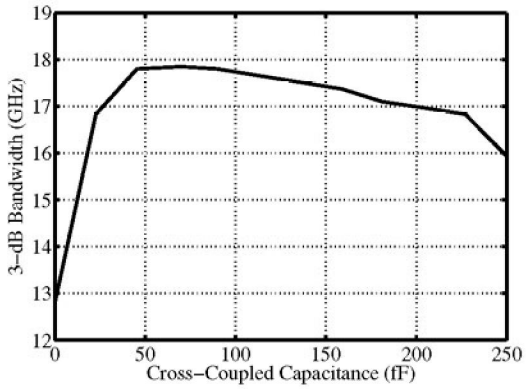



Fig. 2. Simulated bandwidth of the single-ended cascode in Fig. 1(b) showing the effect of cross-coupling capacitance, $C$.

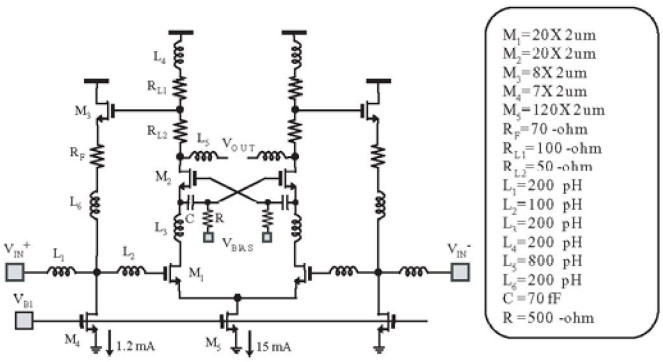



Fig. 3. A broadband differential cascode pre-amplifier with shunt-shunt feedback. All gate lengths are 0.18 $\mu$m.

used for bandwidth improvement. However, if the value of the cross-coupling capacitor, • , is too large, its loading effect at the source of • 2 reduces the bandwidth. Fig. 2 shows simulation results for the single-ended cascode in Fig. 1(b). The component values and bias currents are the same as in the fully-differential pre-amplifier presented in Section III, except that the value of • is swept. They show that by choosing the capacitance correctly (50 – 100 fF, in this case), bandwidth is improved by 5 GHz, greater than 30%, over the case • = 0 (no • $_m$-boosting).

## III. Cascode Pre-Amplifier

This section describes the design of a differential pre-amplifier that employs a • $_m$-boosted cascode in a 0.18-• m CMOS process. A schematic is shown in Fig. 3.

It employs all of the bandwidth enhancement techniques described in Section II in a differential amplifier with shunt-shunt feedback. The cross-coupling capacitance is 70 fF. To accommodate source-follower • 3 in the feedback path, a relatively high supply voltage of 2.5 V was used. Splitting the load resistance into two parts, • $_{L1}$ and • $_{L2}$ reduces the loading effect of the gate of • 3 [9]. Inductors • 1 and • 2 form a passive ladder network to distribute the parasitic capacitances at each node [3]. Finally, the inclusion of • 6 in the feedback path is known to improve bandwidth [10]. The pre-amplifier circuit consumes 44 mW.

The pre-amplifier was fabricated and tested on-wafer. A die photo is shown in Fig. 4(a). The area is 1.4 mm × 0.7 mm. The simulated and measured • 21 of the circuit are plotted on Fig. 5. The measured

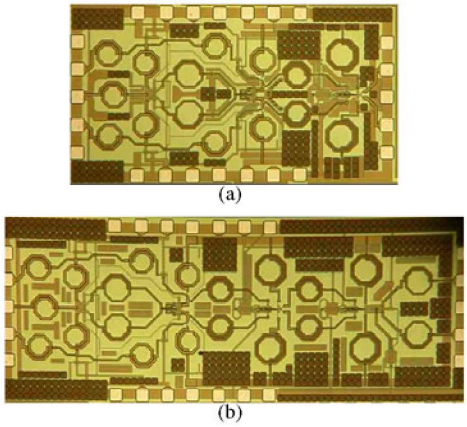



Fig. 4. Die photo of the two fabricated amplifiers: (a) pre-amplifier, (b) complete amplifier.

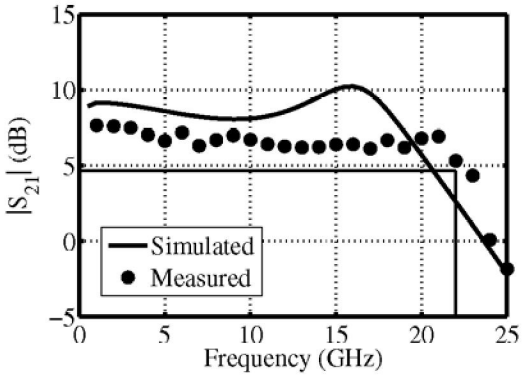



Fig. 5. Measured and simulated $|S_{21}|$ of the differential cascode pre-amplifier. (Single-ended $S_{21}$ was measured and 6 dB added.)

dc gain is 1.5 dB less than simulated. The measured 3-dB bandwidth is 22 GHz with no peaking (20 GHz simulated).

## IV. Complete Amplifier

The complete amplifier comprises the input pre-amplifier described in Section III plus two additional gain stages, as shown in Fig. 6. A schematic of the two post-amplifier gain stages is shown in Fig. 7.

The post-amplifier gain cells employ peaking inductors • 1 and • 2 to increase their bandwidth. In [11], these inductor were chosen so that • 2•• 1 = 2 resulting in 22-GHz bandwidth and a peaked magnitude response. Here, the inductors values were chosen to maintain a flat response and constant group delay, resulting in • 2•• 1 ratios between 0.4 and 0.9, similar to the design in [12]. In addition,

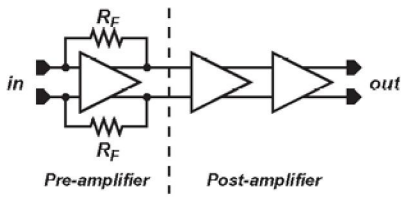



Fig. 6. Block diagram of the complete prototype amplifier.

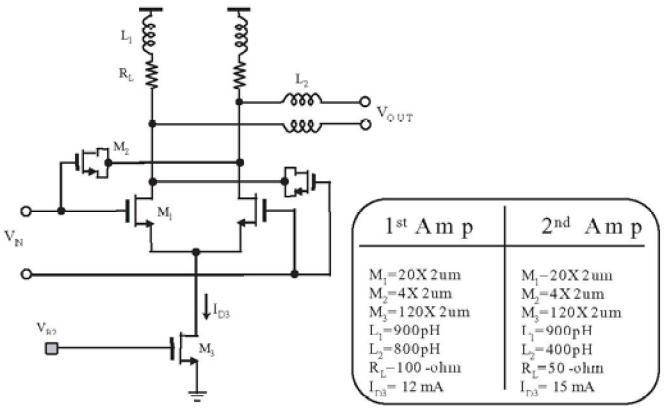



Fig. 7. The post-amplifier gain stages. All gate lengths are 0.18 $\mu$m.

cross-coupled MOS capacitors • 2 serve to partially cancel the gate-drain capacitances of the differential pair devices • 1.

A die photo of the complete amplifier is shown in Fig. 4(b). The total area is 2 mm × 0.7 mm and the total power consumption is 111 mW from a 2.5-V supply. All measurements were performed on-wafer.

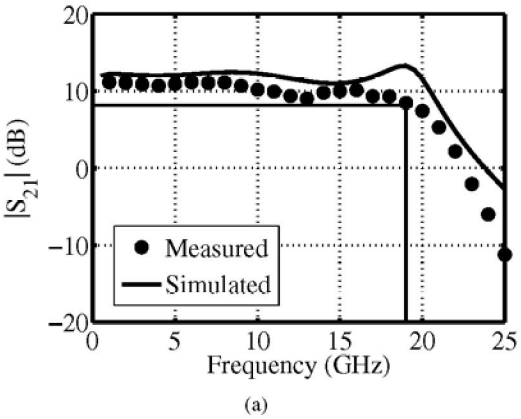
Fig. 8(a) shows the magnitude of • 21 for the complete amplifier, both simulated and measured. The measurements were made with a 2-port network analyzer, so 6 dB was added to show the differential gain. The measured 3-dB bandwidth is 19 GHz with a gain of 11 dB. No peaking is observed in the measured response. The phase response, simulated and measured, is plotted in Fig. 8(b). The phase response is linear, implying constant group delay, within band. Fig. 9 plots the input and output return losses, • 11 and • 22. Since a 2-port network analyzer was used, the results are single-ended. An input return loss better than 9 dB is observed up to 18 GHz, and the output return loss is better than 10 dB from 6 to 16 GHz. If used as the front-end of an integrated receiver, the amplifier will only drive on-chip loads and the output return loss is not critical. The measured transimpedance gain is 52 dBΩ.

To demonstrate the suitability of the amplifier for broadband receiver front-ends, the circuit was tested with NRZ binary data inputs. The inputs are formed by multiplexing together four independent PRBS patterns. In Fig. 10, four $(2^{31}-1)$ PRBS patterns are multiplexed resulting in a length-$4(2^{31}-1)$ pattern. The data rates are 20 and 24 Gb/s and the input swing is 270 mVpp. Only one side of the differential output is shown. The eye patterns are very symmetric with no obvious overshoot. The output eye amplitudes are 400 mVpp per side and the RMS jitter is less than 3 ps.

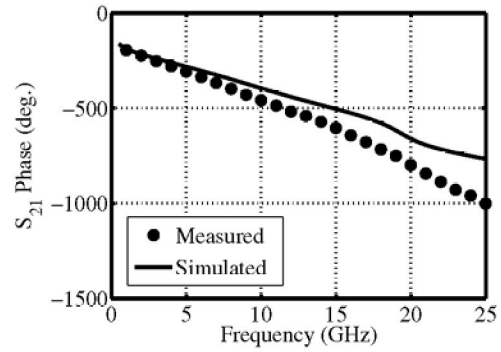
As a sensitivity test, a 20-dB attenuator was used to provide a nominal 27 mVpp input swing. The data rate was decreased to 14 Gb/s to stay within the bandwidth of the attenuator and the pattern length was reduced to $4(2^7-1)$ to accommodate the oscilloscope's pattern locking capability. Fig. 11 shows the eye diagram at the amplifier output and the corresponding bathtub curve, indicating plenty of margin.

## V. Conclusion

A • $m$-boosting technique using capacitive cross-coupling was used to increase the bandwidth of a CMOS cascode stage. The technique was used in the design of a pre-amplifier with a measured 3-dB bandwidth of 22 GHz in a 0.18-• m CMOS process. The pre-amplifier is the first stage of a broadband receiver front end with 11-dB gain, 19-GHz bandwidth, no peaking and linear phase response. These results are summarized in Table I and compared with other recently reported broadband amplifiers based on CMOS cascodes, demonstrating a significant bandwidth improvement. Eye diagrams up to 24 Gb/s show little or no overshoot and excellent symmetry.




(a)




(b)

Fig. 8. Simulated and measured $S_{21}$ of the complete amplifier: (a) magnitude and (b) phase. (Single-ended $S_{21}$ was measured and 6 dB added.)

## Acknowledgments

Thanks to Shahriar Shahramian for his help testing this circuit. This work has been supported by Intel Corporation. CAD tools and fabrication services have been provided by the Canadian Microelectronics Corporation and test facilities by the Emerging Communications Technology Institute at the University of Toronto and the Canadian Foundataion for Innovation.

## References

[1] H.-T. Ahn and D. Allstot, "A 0.5–8.5-GHz fully differential CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 985–993, Aug. 2002.

[2] R.-C. Liu, C.-S. Lin, K.-L. Deng, and H. Wang, "Design and analysis of DC-to-14-GHz and 22-GHz CMOS cascode distributed amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1370–1374, Aug. 2004.

[3] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.

[4] A. Bevilacqua and A. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

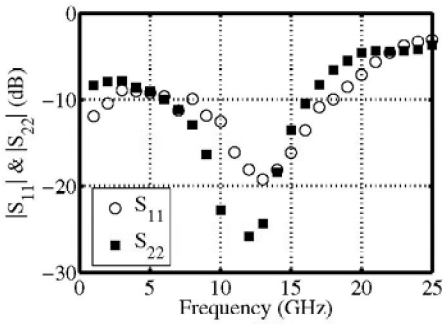
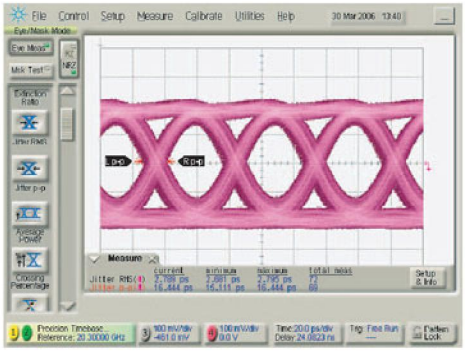
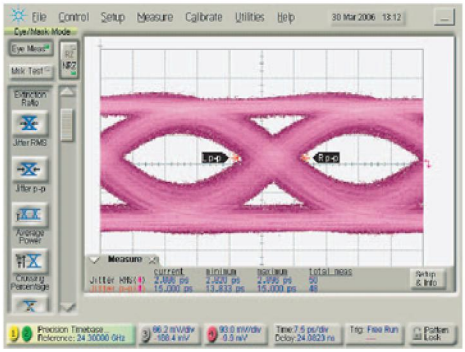



Fig. 9. Measured single-ended input and output return loss of the complete amplifier.

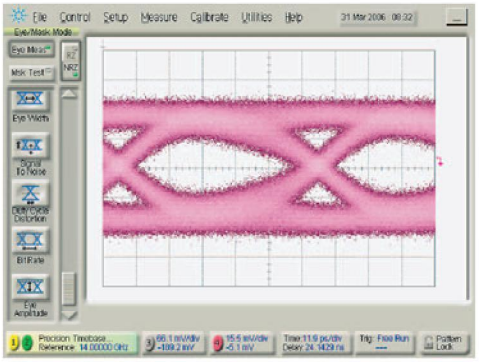


(a)

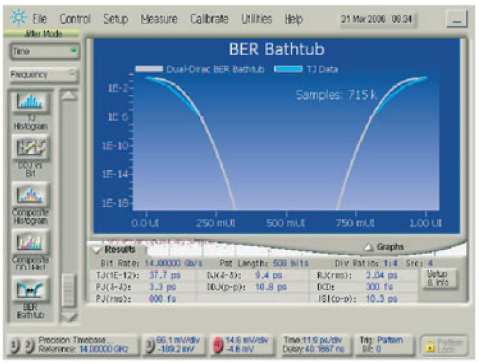


(b)

Fig. 10. Single-ended 400-mVpp output eye diagrams using a length-$4(2^{31}-1)$ 270-mVpp NRZ input data pattern at: (a) 20 Gb/s (b) 24 Gb/s.



(a)




(b)

Fig. 11. (a) Single-ended 60-mVpp output eye diagram for a 27-mVpp input length-$4(2^7-1)$ NRZ pattern at 14 Gb/s. (b) The corresponding BER measurement.

| | **This work** | [3] | [4] |
|---|---|---|---|
| CMOS Technology | 0.18 $\mu$m | 0.18 $\mu$m | 0.18 $\mu$m |
| Single-ended (SE) or Differential (Diff.) | Diff. | SE | SE |
| 3-dB Bandwidth (GHz) | 19 | 9.2 | 7.5 |
| In-band $\lvert S_{21}\rvert$ (dB) | 11 | — | 9.3 |
| In-band $\lvert Z_{21}\rvert$ (dBΩ) | 52 | 54 | — |
| Sensitivity ($\mu$W) | 3.6 @ 14 Gb/s | 15.8 @ 10 Gb/s | — |
| Power (mW) | 111 | 137.5 | 9 |
| Supply voltage (V) | 2.5 | 2.5 | 1.8 |
| Area (mm$^2$) | 1.4 | 0.64 | 1.1 |

TABLE I

PROTOTYPE SUMMARY AND COMPARISON WITH OTHER RECENTLY REPORTED BROADBAND CMOS AMPLIFIERS BASED ON CASCODE STAGES.


[5] W. Zhuo, S. Embabi, J. de Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in rf low noise amplifiers and down-conversion mixer design," in *European Solid-State Circuits Conference*, 2000, pp. 77–80.

[6] X. Li, S. Shekhar, and D. Allstot, "$g_m$-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-$\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[7] E. Sackinger, *Broadband Circuits for Optical Fiber Communication*. John Wiley & Sons Inc., 2005.

[8] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.

[9] Y. Greshishchev and P. Schvan, "A 60-db gain 55-db dynamic range 10-Gb/s broadband SiGe HBT limiting amplifier," in *International Solid-State Circuits Conference*, 1999, pp. 382–383.

[10] H. Tran, F. Pera, D. S. McPherson, D. Viorel, and S. P. Voinigescu, "6-kΩ 43-Gb/s differential transimpedance-liimiting amplifier with auto-zero feedback and high dynamic range," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1680–1689, Oct. 2004.

[11] S. Galal and B. Razavi, "40-Gb/s amplifier and esd protection circuit in 0.18-$\mu$m CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389–2396, Dec. 2004.

[12] K. Kanda, D. Yamazaki, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, and H. Onodera, "40-Gb/s 4:1 MUX/1:4 DEMUX in 90-nm standard CMOS," in *International Solid-State Circuits Conference*, 2005, pp. 152–153.