Coupled loops at 20 GHz for stacked planar circuits

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Differential planar coupled loops are examined as a method of integrating silicon electronics with passive elements on low-loss microwave laminates. Two test structures are examined which abut planar loops on a CMOS chip to similarly sized loops on a low-loss microwave laminate. The insertion loss of a pair of the 1000 × 1000 μm loops was measured to be approximately 3 dB at 20 GHz, and the loss between the 700 × 300 μm loops was measured to be approximately 6 dB at 20 GHz.

Introduction: A recent area of focus has been the development of capacitive and inductive coupling between stacked chips. In contrast with wired flip-chip assembly, wireless interconnects offer lower assembly cost and the ability to test high-speed operation without mechanically affixing the stacked chips [1]. Stacked planar inductors have been used to create inter-chip wireless interconnects using thinned silicon chips [1]. In [2], coupling between stacked inductors was examined using 50 μm diameter inductors with 10 turns, which were fabricated on different layers of the same silicon substrate, for use as AC interconnects. The structures presented approximately 8 dB loss through a single set of coupled inductors at 6 GHz, but used very close metal layers on the same substrate. In this Letter we present low insertion-loss differential coupled loops for the purpose of coupling stacked planar circuits at frequencies around 20 GHz. The structures presented here were designed to test structures that could be used to integrate passive elements on low-loss laminates, such as efficient planar antennas, with silicon electronics.

Test structures: To study the loss encountered by a coupled pair of loops on two different substrates, pairs of symmetric loops were designed and fabricated as shown in Fig. 1. To characterise the loops using two wafer probes on the same layer, two pairs of loops were connected in series, forming the equivalent of two transformers in series, as shown in Fig. 1*a*. The insertion loss of a single pair of loops is approximately half that of these test structures. The two planar substrates used were a 220 μm-thick silicon CMOS chip with a substrate conductivity of approximately 10 S/m from a standard 0.18 μm CMOS process, and a Rogers Duroid 5880 laminate with a thickness of 250 μm.

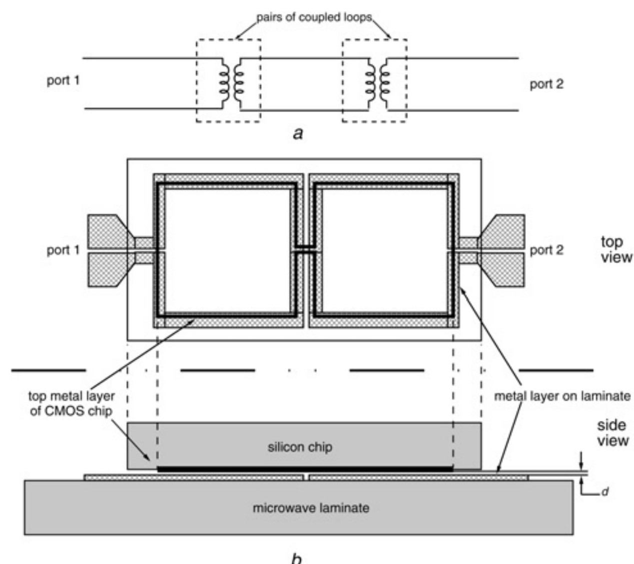

Fig. 1 *Fabricated test structures forming two series connected transformers (Fig. 1a), and test structures (Fig. 1b) consisting of microwave laminate mated to CMOS chip, with adjacent loops on abutting faces forming a transformer (Figure not to scale)*

Three different loop sizes were selected to be representative of loop sizes that could be used to couple silicon electronics with elements on another substrate. The smallest set of loops had dimensions of 700 × 100 μm for each loop, the medium loops had dimensions of 700 × 300 μm, and the large loops were 1000 × 1000 μm each. Although the largest loops occupy a significant area on the silicon chip, it will be shown that metal can be placed inside these loops, providing the opportunity to place loops around silicon electronics.

The loops were designed and simulated using a method-of-moments simulator. Based on these simulations, the large loops on the CMOS chip were chosen to have a 40 μm linewidth, and the loops on the microwave laminate were chosen to have a linewidth of 85 μm for optimum coupling at frequencies around 20 GHz.

A photograph of the fabricated CMOS chip is shown in Fig. 2. The largest loop pairs on the laminate are shown at the bottom of Fig. 2. Similar structures using the medium and small loop dimensions were also fabricated on the laminate, but are not shown. To conserve space on the CMOS chip, the small loops were placed inside of the larger loops, and additional metal was placed around the loops to conform to metal density requirements specified by the CMOS foundry design rules. The layout of loops inside one another, and addition of metal fill, did not significantly affect the properties of the loops in simulation compared to isolated loops.

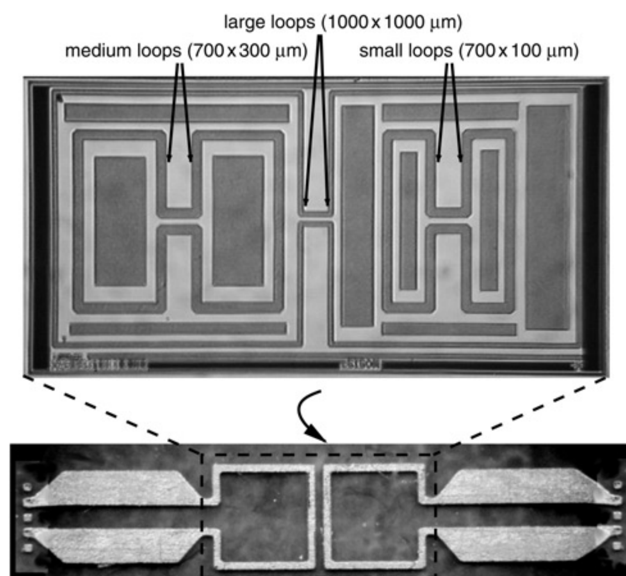

Fig. 2 *Photograph of loops fabricated on CMOS chip (top), and test structure using 1000 × 1000 μm loops on microwave laminate (bottom)*

Extra metal on CMOS chip is metal fill required by CMOS foundry

Measurements: The silicon chip was placed on the laminate and positioned using a pin on a simple micropositioner. The spacing between loops was set primarily by the planarity of the laminate, and is estimated to be of the order of 10 μm, based on simulations. The spacing is consistent between test structures, as estimated by comparing the measured insertion losss. For these test structures the layers were not joined with an adhesive, allowing the silicon chip to be moved relative to the laminate using the micropositioner. However, measurements of similar test structures joined with a delayed-adhesion ethyl cyanoacrylate adhesive yielded similar results to those reported here.

S-parameters of the structures were measured using two differential ground-signal-ground microwave probes. Four-port single-ended S-parameters were converted to differential two-port S-parameters using mixed-mode equations [3]. Fig. 3*a* shows the measured differential-mode S-parameters of the large paired 1000 × 1000 μm coupled loops, and Fig. 3*b* shows the measured data for the medium sized loops. The variation in insertion loss over the bandwidth from 10–25 GHz is partly due to impedance mismatches between the two loops which would not be present in a single pair of coupled loops. The measured data show the same behaviour as simulations, though the ripple in the measured insertion loss from 10–25 GHz is less than the ripple in simulation. The difference is most likely due to the uncertainty in the gap thickness and planarity. The results for the 700 × 100 μm loops are not shown, as the insertion loss of that structure is around 20 dB.

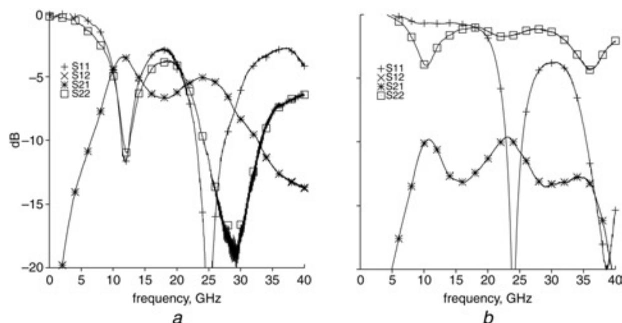

Fig. 3 *Measured differential S-parameters of structure with 1000 × 1000 µm loops and 700 × 300 µm loops*

a 1000 × 1000 µm loops
b 700 × 300 µm loops
Insertion loss of single pair of stacked inductors would be approximately half the insertion loss shown here for two series connected stacked pairs

The loss of a single coupled loop structure, consisting of a single loop on the silicon chip and a single loop on the microwave laminate, is approximately one half of the insertion loss of these test structures. This would give an insertion loss of approximately 3 dB from 10 to 20 GHz for 1000 × 1000 µm loops, and 6 dB at 20 GHz for 700 × 300 µm loops. It should be noted that these networks were not impedance matched, and so the insertion loss could be improved by the addition of impedance matching networks over the frequency range of interest.

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