A Programmable Phase Rotator based on Time-Modulated Injection-Locking

Frank O'Mahony[1], Bryan Casper[1], Mozhgan Mansuri[1] and Masum Hossain[2]

[1]Intel Corporation, Hillsboro, OR, USA · Tel: 1-503-712-2992 · Email: frank.omahony@intel.com
[2]Department of Electrical and Computer Engineering, University of Toronto, Canada

Abstract

A 7-bit 360° phase rotator in 45nm CMOS interpolates between coarse phases by modulating the injection point of an oscillator. This architecture decouples phase resolution from device sizing. INL and DNL are improved by independently adapting the delay of each oscillator stage. A digital phase-locked loop using a time-to-digital converter based on a tracking ADC keeps the oscillator tuned to the injection frequency. The measured DNL and INL at 4.05GHz with phase calibration are 0.4 and 1.2 LSBs, respectively, while consuming 14.3mW.

Keywords: phase rotator, injection locked oscillator, I/O

Introduction

A digitally programmable phase rotator (PR) is a key component for many wireline I/O architectures. Most conventional PRs achieve fine phase step resolution by interpolating between coarse phases using static DACs. The resolution of these PRs can be improved by reducing the LSB device size or bias voltage. However, both of these options cause variation to increase, leading to larger phase step errors.

PRs based on injection-locked oscillators (ILOs) have the advantage of filtering the clock jitter without requiring an explicit control loop. In [1], an LC-ILO adjusts the clock phase by tuning the tank resonant frequency. However, the tuning range is less than 360° and the jitter filtering bandwidth is a function of phase. In [2], infinite phase rotation is achieved by interpolating the injection point into a ring oscillator. However, because the phase interpolation uses static DACs, it exhibits the tradeoff between resolution and variation or power.

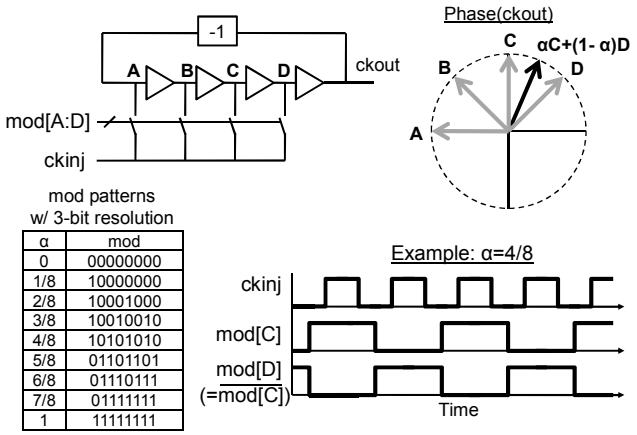
This paper describes a 7-bit 360° PR that uses time-modulated injection rather than DACs to interpolate between coarse phases. INL and DNL due to deterministic error or random variation are improved by optimizing the delay of each oscillator stage. The tuned frequency of the ILO tracks the injected clock using a digital PLL and replica ILO.

Design overview

A. Phase rotator

The PR concept is shown in Fig. 1. The phase of *ckout* relative to *ckinj* is determined by the injection point. Phase interpolation between coarse phases (e.g. phases C and D) is achieved by time-modulating the injection point. Because of the dynamic injection point, the effective jitter amplitude of the injection clock is equal to the coarse phase spacing. However, the ILO has a low-pass jitter transfer characteristic which attenuates modulation jitter. Even so, jitter on *ckout* due to the dynamic injection point will be proportional to the coarse phase spacing. This time-modulated phase interpolation is similar to the approach proposed for a PLL-based PR in [3].

The actual implementation of this concept is shown in Fig. 2. It consists of a 4-stage differential ring oscillator with injection points between each stage. The clock is injected into the oscillator through 5fF metal capacitors. This eliminates static current into the disabled injection points. It also provides low



α	mod
0	00000000
1/8	10000000
2/8	10001000
3/8	10010010
4/8	10101010
5/8	01101101
6/8	01110111
7/8	01111111
1	11111111

Fig. 1 Phase rotator concept with time-modulated injection point.

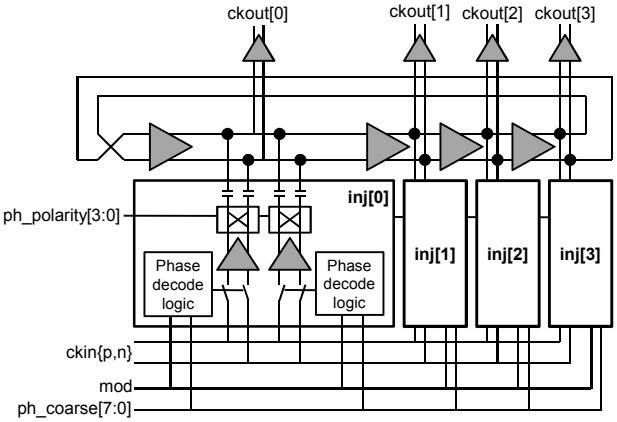


Fig. 2 Four-stage ring ILO with time-modulated injection point.

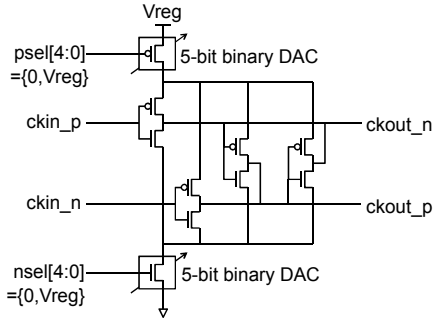


Fig. 3 Oscillator delay stage with programmable delay.

injection strength even though the per-node injection buffer drive strength is identical to that of the oscillator stages. Each injection buffer is segmented into two independent paths. For each phase code, one injection buffer is always enabled while its two adjacent neighbors are modulated. This effectively doubles the number of coarse phase settings and reduces the jitter due to injection-point modulation by a factor of two. A decoder within each injection segment interprets the digital coarse phase setting (*ph_coarse*) and modulation signal (*mod*).

The oscillator delay stages are pseudo-differential inverters with a regulated supply (Fig. 3). The buffer delays are independently tunable by adjusting 5-bit pMOS and nMOS resistor DACs. The delay of the stages can be adjusted to minimize

INL and DNL due to deterministic and random nonidealities.

B. Complete system with frequency tracking loop

The complete PR schematic is shown in Fig. 4. It includes the phase rotating ILO (ILO_PR), clock predrivers, an 8-bit coarse frequency DAC and two shift registers (SRs). The SRs loop the 8-bit programmable phase modulation patterns and operate at the injected clock frequency. With two SRs, the phase code can be updated by changing which SR pattern is sent to ILO_PR rather than stopping the SR to load in a new pattern.

The PR also includes a digital PLL with an identical replica ILO (ILO_REP). This loop biases the ILOs so that their free-running frequency tracks the injected clock. Untracked frequency drift would otherwise cause phase drift at the output of the ILO [1]. The loop operates by adjusting the bias voltage, *Vreg*, such that the injection clock phase tracks the output phase of ILO_REP. Since there is a proportional relationship between frequency offset and the ILO phase delay, the phase-locked condition also forces the frequencies to track. Unlike ILO_PR, ILO_REP has a fixed injection point.

The feedback loop consists of a time-to-digital converter (TDC), a digital loop filter, three current-mode DACs (IDACs), and a capacitor. The 5 LSBs of the integral path output feed a second-order delta-sigma modulator (DSM) and 3-level IDAC to improve the frequency resolution. All IDACs are fully thermometer coded. The TDC (Fig. 5) is based on a tracking ADC. The binary phase detector (!!PD) output feeds an integrator. The integrator output increments the offset of the phase detector in the same direction as the residual phase error. The integrator output code therefore provides a 5-bit measure of the phase error. The !!PD is a modified StrongArm latch wherein the two clocks gate the left and right device stacks. Resistor DACs adjust the phase offset (*offset*) and phase step size (*kfix*). The nominal phase resolution of the TDC is <1ps.

Measured results

The complete PR in Fig. 4 was implemented in a 45nm digital CMOS process. The measurement results are at room temperature with a 1.0V power supply and a 4.05GHz injected clock. The digital PLL correctly tracks the injection clock frequency based on observation of the PLL integrator output. Per-stage delay is optimized using a software-defined algorithm that minimizes the measured INL at the coarse phase codes. The pre- and post- optimized phase linearity and jitter are shown in Fig. 6. Including per-stage delay optimization, the measured DNL and INL are 0.4 LSB (1.1°) and 1.2 LSB (3.4°), respectively. The optimized DNL and INL are 52% and 48% lower than the initial un-optimized results. As expected, jitter varies as a function of phase code, with minimums when the modulation pattern is all 0's or 1's. The total jitter ranges from 0.7 to 1.7ps-rms. The complete PR consumes 14.3mW, including 10.6mW for the predriver, ILOs and ILO phase buffers, 1.1mW for the SR and phase decoder logic (with "10101010" pattern), and 2.6mW for the digital control loop. Excluding test circuitry, it occupies 0.08mm^2.

Acknowledgements

The authors thank Ganesh Balamurugan, James Jaussi, Joe Kennedy, Clark Roberts, Sudip Shekhar, Neal Tanksley, Valerie Baca, David Wu, Jason Howard, Howard Wilson, David Finan and David Jenkins for contributions to this work.

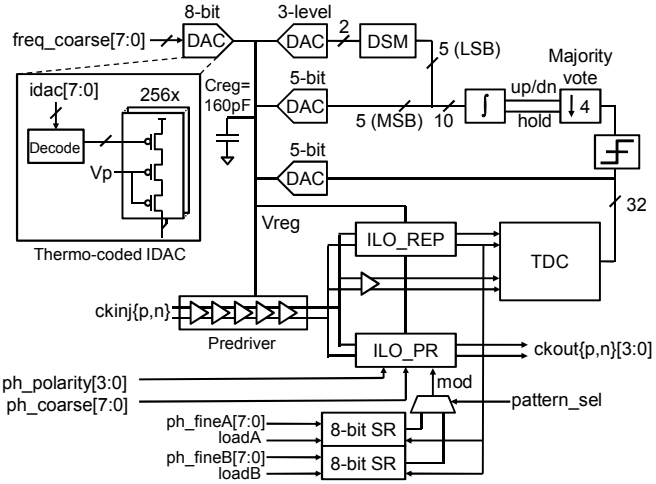


Fig. 4 Implemented phase rotator and ILO phase-locked loop.

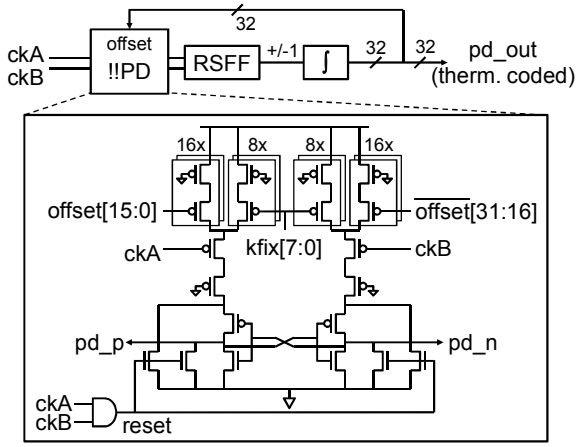


Fig. 5 Time-to-digital converter based on a tracking ADC.

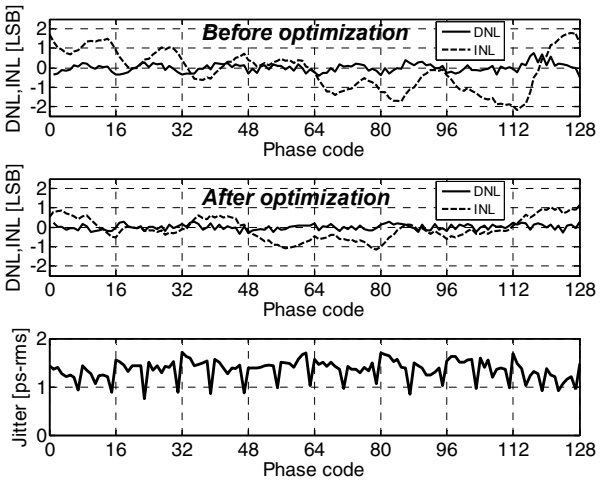


Fig. 6 Measured DNL, INL, and jitter across one clock period (128 codes) at 4.05GHz.

References

[1] F. O'Mahony, et al., "A 27Gb/s Forwarded-Clock I/O Receiver Using an Injection-Locked LC-DCO in 45nm CMOS," in *ISSCC 2008 Digest of Tech. Papers*, pp. 452-453.

[2] H.-T. Ng, et al., "A second-order semidigital clock recovery circuit based on injection locking", *IEEE J. Solid-State Circuits*, vol. 38, pp. 2101-2110 , Dec. 2003.

[3] P. Hanumolu, G.-Y. Wei, and U.-K. Moon, "A wide tracking range 0.2-4Gbps clock and data recovery circuit," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2006, pp. 88-89.