# A 40-Gb/s Serial Link Transceiver in 28-nm CMOS Technology

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## Abstract

A SerDes operating at 40 Gb/s optimized for chip-to-chip communication is presented. Equalization consists of 2-tap feed-forward equalizers (FFE) in both transmitter and receiver, a 3-stage continuous-time linear equalizer (CTLE) and discrete-time equalizers including a 17-tap decision feedback equalizer (DFE) and a 3-tap sampled-FFE in the receiver. The SerDes is realized in 28-nm CMOS technology with 23.2 mW/Gb/s power efficiency at 40 Gb/s.

## Introduction

I/O bandwidth requirements of communication systems such as routers and backplane based servers are growing rapidly due to the demand of networking and cloud-based applications. While electrical signaling over copper channels is still the favorable choice of many interconnects, numerous challenges are imposed in high-speed CMOS transceiver design [1-3]. This paper demonstrates a 40-Gb/s SerDes using NRZ signaling with the capability of compensating 20-dB loss at half baud-rate. The prototype consists of four 40-Gb/s Tx/Rx pairs and two clock generation units. Several equalization techniques such as FFE, CTLE, and DFE are adopted to combat channel loss and limited circuit bandwidth.

## Transceiver Architecture

Fig. 1 shows the block diagram of the transceiver. The transmitter uses a current mode driver with one tap pre-emphasis that can be programmed to compensate either 1st pre- or post-cursor ISI. Shunt inductive-peaking is used in the last-stage 2-to-1 multiplexer and a T-coil network is used at the final driver to further extend the circuit bandwidth.

While it is essential to apply ESD protection to the silicon, the bandwidth loss due to ESD parasitic capacitance and termination resistance is too large. The receiver front-end shown in Fig. 2 implements a distributed ESD topology [4] to minimize the impact of parasitics on input bandwidth and achieve good return loss. The inductors and ESD loading create an LC delay line tuned to ~20-ps total delay allowing a 2-tap transversal filter to cancel either pre- or post-cursor ISI. The following CTLE is composed of a two-stage active feedback amplifier and a peaking buffer with a T-coil to drive the loading of the DFE and CDR inputs. The proposed active feedback amplifier takes advantage of Miller effect to increase the effective inductance and can achieve larger peaking at high frequency compared to a conventional feedback connection as shown in Fig. 2(b)(c).

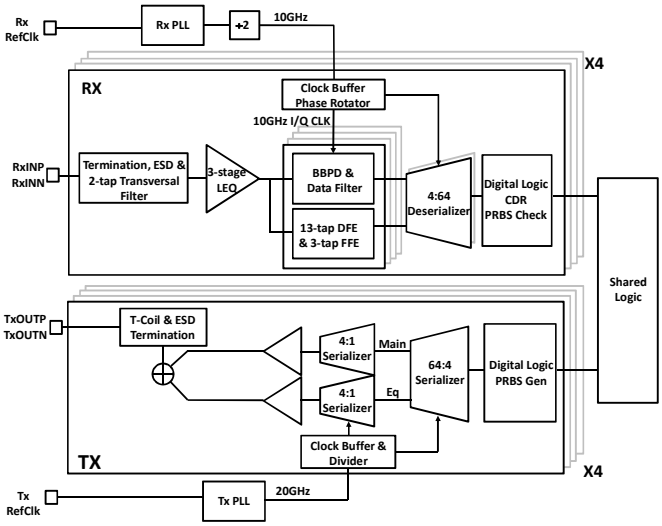


Fig. 1. Transceiver block diagram.

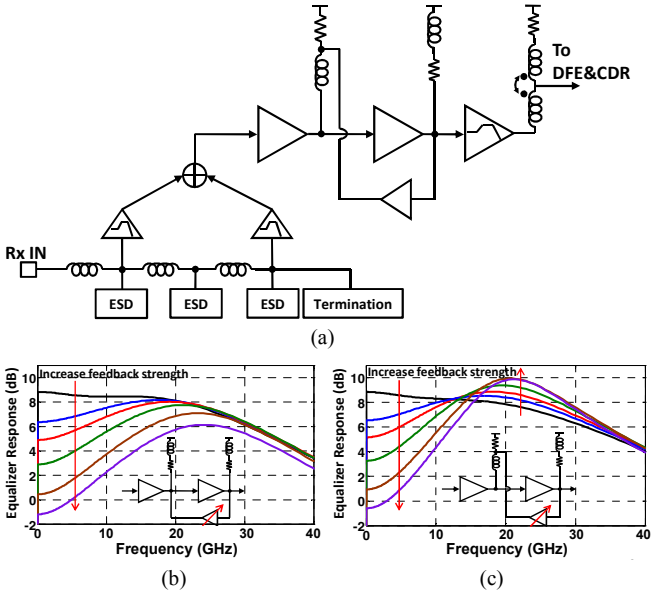


Fig. 2. (a) Block diagram of receiver analog front-end, and the simulated frequency response of (b) conventional and (c) proposed active feedback equalizer with inductive-peaking.

The hybrid discrete-time equalizer in the receiver contains a 3-tap sampled-FFE and a 17-tap DFE operated at quarter rate as shown in Fig. 3. Integrate-and-hold stages similar to [5,6] are used to generate static output in hold mode for the succeeding samplers to relax their aperture requirement. Although loop-unrolling technique is used for the 1st post-tap, the feedback for the 2nd post-tap is still very challenging at such high data rates. Instead of using 2-tap loop unrolling, two integrate-and-hold stages are cascaded to provide larger gain and create sampled-delay for FFE operation. The signal is delayed by 2 UI and used for 2nd post-cursor as well as pre-cursor cancellation. In addition to the loop-unrolling DFE for the 1st tap, dynamic feedback data are applied to cancel 3rd-14th post-cursor ISIs. Floating taps are also implemented to cover any consecutive four taps ranging from 15th-30th post-tap position to minimize possible long tail or channel reflection effects. Both clock duty cycle and quadrature correction as well as sampler offset cancellation are applied to minimize the mismatch between four interleaving paths.

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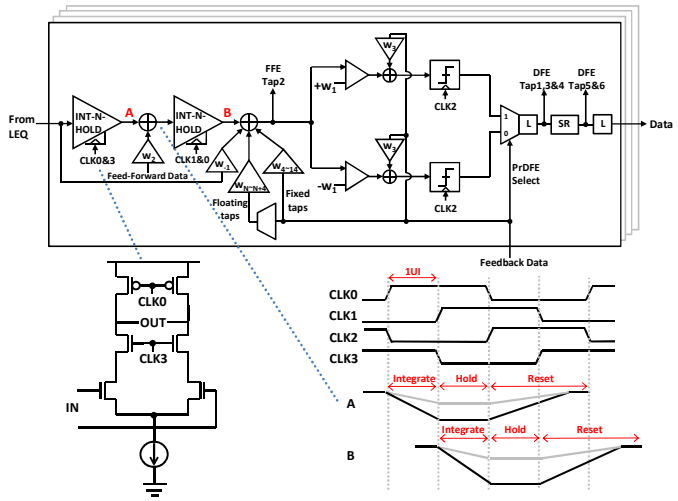



Fig. 3. Hybrid discrete-time equalizer with 3-tap sampled-FFE and 17-tap DFE.

Two PLLs are implemented, with Tx and Rx sides each sharing a PLL. This approach provides short high-speed clock distribution and larger frequency tracking capability through the use of a Fractional-N PLL in addition to the typical digital CDR in the receiver [7] with less than 10% power and area penalty.

## Measurement Results

A quad SerDes is fabricated in a 28-nm CMOS process whose micrograph is shown as Fig. 4. The area of a single transceiver pair with PLL overhead amortized is 0.81 mm$^2$. The chip is powered with 0.85 V and 1.1 V supplies and the power per Tx/Rx lane is 927 mW at 40 Gb/s, including PLL and clocking overheads. The measured PLL random jitter is 170 fs (rms) in the 10 MHz-to-10 GHz band. Fig. 5 shows the transmitter output eye diagrams after an 8-dB loss channel (ESD devices and termination add another 4-dB loss at 20 GHz). Tx-FFE is applied for post-cursor cancellation in order to obtain an open eye. Fig. 6 shows the transceiver performance over a 12-inch PCB trace with total 20-dB loss at 20 GHz including PCB & package substrate but not on-chip ESD losses. The received post-equalized eye captured by an on-chip eye monitor has a horizontal eye opening of 0.27 UI at BER=$10^{-9}$ with 40-Gb/s PRBS31 pattern. The extrapolated eye opening at BER=$10^{-15}$ is 45 mV by 0.15 UI.

## Conclusion

This paper presents a fully-integrated quad serial link transceiver in 28-nm CMOS operating at 40 Gb/s per lane. Distributed ESD with transversal filter, CTLE with an active feedback peaking amplifier, and a hybrid discrete-time equalizer with sampled-FIR and DFE are used in the receiver.

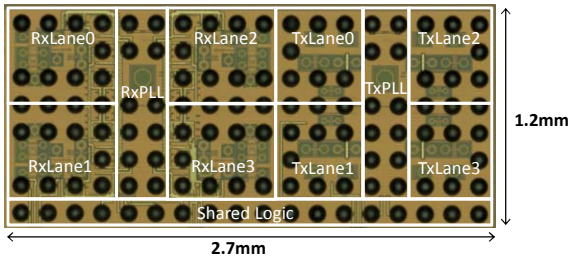
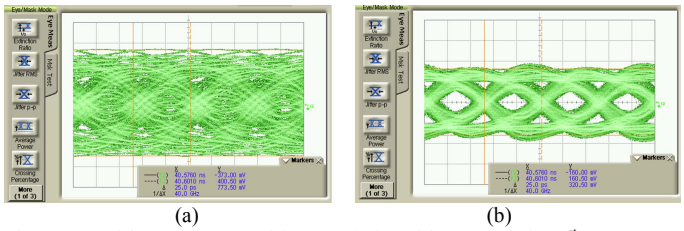
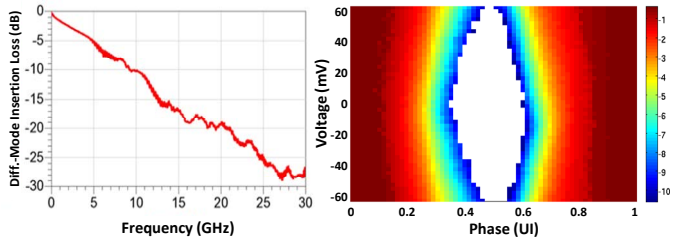



Fig. 4. Micrograph of the 4 lane SerDes.



(a) (b)

Fig. 5. 40-Gb/s Tx eye (a) without and (b) with Tx-FFE for 1st post-cursor cancellation after an 8-dB loss channel.




(a) (b)

Fig. 6. (a) Frequency response of 12-inch PCB trace and package substrate. (b) Post-equalized BER eye at receiver data samplers with 40-Gb/s PRBS31 data pattern.

The transceiver demonstrates a 40-Gb/s error free operation (BER<$10^{-15}$) over a channel with 20-dB loss. Table I summarizes the performance of the transceiver in comparison with other recently published high-speed SerDes devices.


## Acknowledgment

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TABLE I

PERFORMANCE SUMMARY

| | [2] | [3] | This Work |
|---|---|---|---|
| Technology | 32nm SOI CMOS | 40nm CMOS | 28nm CMOS |
| Data Rate | 28 Gb/s | 28 Gb/s | 40 Gb/s |
| TX Equalization | 3-tap FFE | 3-tap FFE | 2-tap FFE |
| RX Equalization | CTLE and 15-tap DFE | CTLE | 2-tap transversal filter, CTLE, 3-tap sampled-FFE, and 17-tap DFE |
| Area/Lane | 0.81 mm$^2$ | 0.9 mm$^2$ | 0.81 mm$^2$ |
| Random Jitter(rms) | 250 fs | 150 fs * | 170 fs |
| Channel Loss | 35 dB ** | 13 dB | 20 dB ** |
| Power/lane | 693 mW | 225 mW | 927 mW |
| Energy Efficiency | 24.8 mW/Gb/s | 8 mW/Gb/s | 23.2 mW/Gb/s |

*Integrate up to 1GHz **Includes package